

02-25-04
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22511 7590 11/28/2003
**ROSENTHAL & OSHA L.L.P.
1221 MCKINNEY AVENUE
SUITE 2800
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/980,891	12/03/2001	Masahiro Ishida	02008.071001; AD-0243PCTU	1563
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TITLE OF INVENTION: METHOD AND APPARATUS FOR DEFECT ANALYSIS OF SEMICONDUCTOR INTEGRATED CIRCUIT

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
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nonprovisional	NO	\$1330	\$300	\$1630	03/01/2004
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EXAMINER	ART UNIT	CLASS-SUBCLASS
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NGUYEN, TUNG X	2829	324-765000
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Advantest Corporation

Tokyo JAPAN

Please check the appropriate assignee category or categories (will not be printed on the patent); ☐ individual ☒ corporation or other private group entity ☐ government

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2/24/04

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03/01/2004 MBELETE2 00000058 09980891

01 FC:1501
02 FC:1504
03 FC:8001

1330.00 OP
300.00 OP
12.00 OP

CERTIFICATE OF MAILING BY "EXPRESS MAIL" (37 CFR 1.10) Applicant(s): Masahiro ISHIDA, et al.			Docket No. 02008.071001; AD-0243PCTUS	
Serial No. 09/980,891	Filing Date 12/03/2001	Examiner T. X. Nguyen	Group Art Unit 2829	
Invention: METHOD AND APPARATUS FOR DEFECT ANALYSIS OF SEMICONDUCTOR INTEGRATED CIRCUIT				
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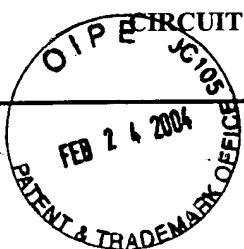
TRANSMITTAL OF PAYMENT OF ISSUE FEE (Large Entity)
(37 C.F.R. 1.311)

Docket No.
02008.071001; AD-0243PCTUS

Applicant(s): Masahiro ISHIDA, et al.

Serial No.	Filing Date	Examiner	Group Art Unit	Confirmation No.
09/980,891	12/03/2001	T. X. Nguyen	2829	1563

Invention: **METHOD AND APPARATUS FOR DEFECT ANALYSIS OF SEMICONDUCTOR INTEGRATED**




Mail Stop Issue Fee
TO THE COMMISSIONER FOR PATENTS
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- ☒ Issue Fee Transmittal Form PTOL-85
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Dated: 2/24/04

 #45,079
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